# Opto-Electronic Technology at its Best: SASER-Horizontal

**Three SASER (Safe and Secure European Routing) cross cutting sub-projects developed a common optical/electronic technology and component base as well as test infrastructure for the three SASER system sub-projects SASER-SaveNet, SASER-Siegfried and SASER-ADVAntage-Net. These sub-projects were "Optical Components", led by Finisar Germany, "Efficient Electronic Converters", led by Socionext and "Test Infrastructure and System Tests", led by Deutsche Telekom T-Labs. The results were far beyond the current state of the art in opto-electronic components, leading to a significant European technology push in this area. Projects like SASER-Horizontal are crucial for Europe's companies, because they ensure that technology invented and made in Europe stays at the competitive edge necessary to be successful in the global market of cutting edge technical products.**

## 1 Optical Components Sub-Project

The opto-electronic components and integrated optics of the sub-project "Optical Components" are key building blocks for next generation energy efficient, flexible and reliable optical systems based on software defined coherent transponders and advanced error correction coding schemes for adaptive, safe and reliable data transport. A high level of component and subsystem integration is the basis to achieve stable operation of these adaptive systems. Therefore compact semiconductor-based optical components were developed in the InP- and GaAs-based material system for short-term, and integrated optics based on silicon-photonics for the long term.

The target specifications of the components under development, i.e. tuneable cw-lasers, highly-integrated modulators and receivers, were defined jointly by the system partners together with the partners of this sub-project. Based on these specifications, the sub-project researched and developed novel concepts and opto-electronic components in different material systems, for different target applications, volumes and prize scenarios, as well as different time frames for commercialization.

In the following we present some of the main prototypes made available by the sub-project:

### 28 / 56 Gbaud InP receivers with and w/o amplifier

- Coherent receiver bandwidth up to 47 GHz
- Monolithic integrated dual-polarisation 90° hybrids and PDs
- Hybrid integrated polarization beam splitter, VOAs and monitors

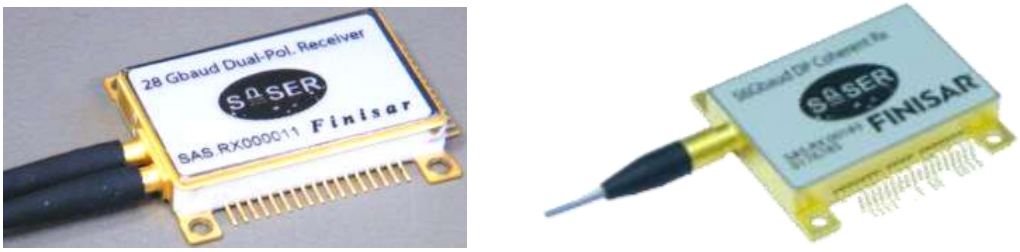



*Fig. 1: Small form factor 28Gbaud dual-pol. coherent receiver (left), 56Gbaud dual pol. coherent receiver (without electrical amplifier) (right)*

## Complex InP and GaAs modulators w/o hybrid integrated driver

- Complex InP modulator PICs with hybrid integrated SiGe drivers
- Integrated SSB functionality offers two channels / wavelengths per chip
- 100Gbps (QPSK) or 200Gbps (16QAM) per channel, totalling to 400Gbps per module
- Differential 25 Ohm termination for low power consumption

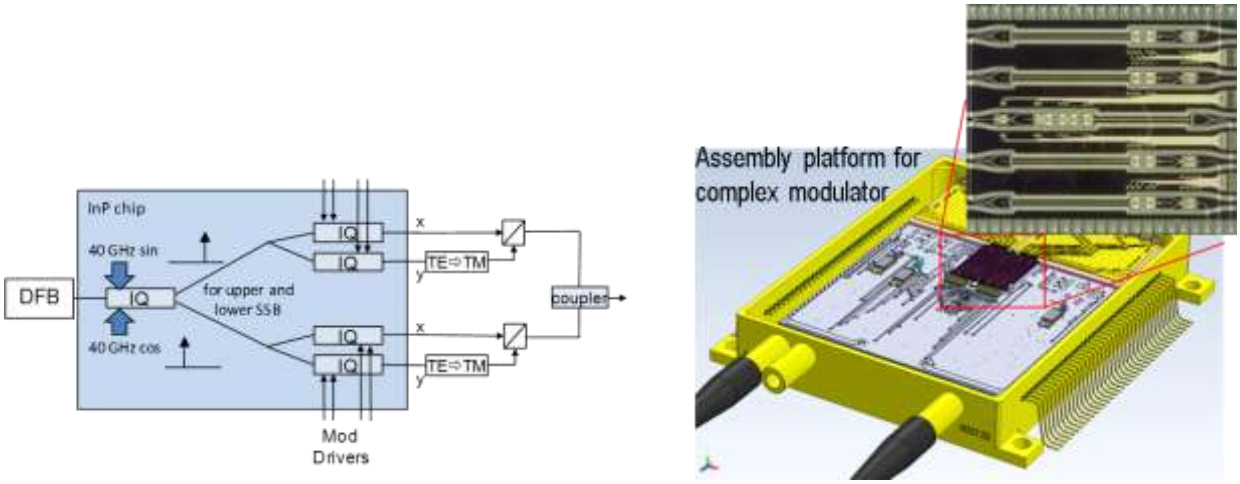



*Fig. 2: Fully integrated dual-carrier dual-polarization I/Q modulator with SiGe driver electronics. Chip schematic (left), manufactured chip and package concept (right)*

- InP modulators with segmented electrodes and hybrid integrated SiGe-driver arrays
- $V_\pi \leq 1V$ and Bandwidth > 40GHz
- Compensation of non-linear MZ transfer function or integration of an purely optical DAC functionality

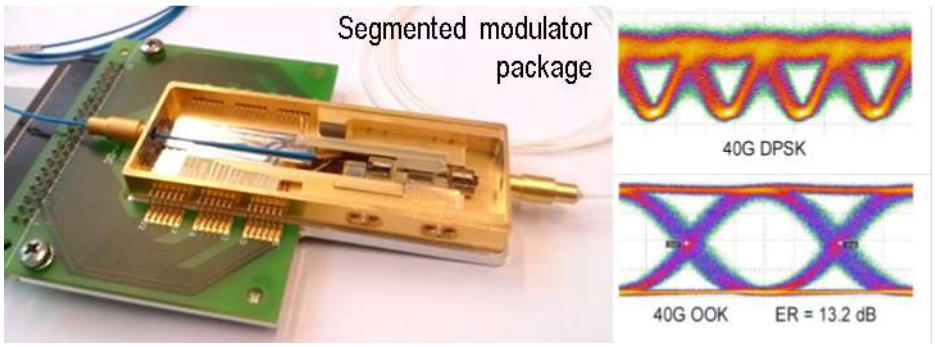



*Fig. 3: Packaged segmented InP I/Q modulator with and SiGe electronics (left), 40G DPSK and 40G OOK eye diagrams of the initial module (right)*

- 28 / 56Gbaud Dual-Polarisation I/Q modulators in GaAs
- State-of-the-art performance (IL < 8dB; BW > 30 GHz)
- Successfully tested at 16 QAM

*Fig. 4: Packaged 28Gbaud Dual-Pol. I/Q modulator in GaAs*

## C-band tuneable high-power cw-laser development

- Hybrid integrated tuneable cw-laser (InP gain chip, polymer grating)
- Monolithically integrated tuneable cw Quantum Dot-laser (InP QD)

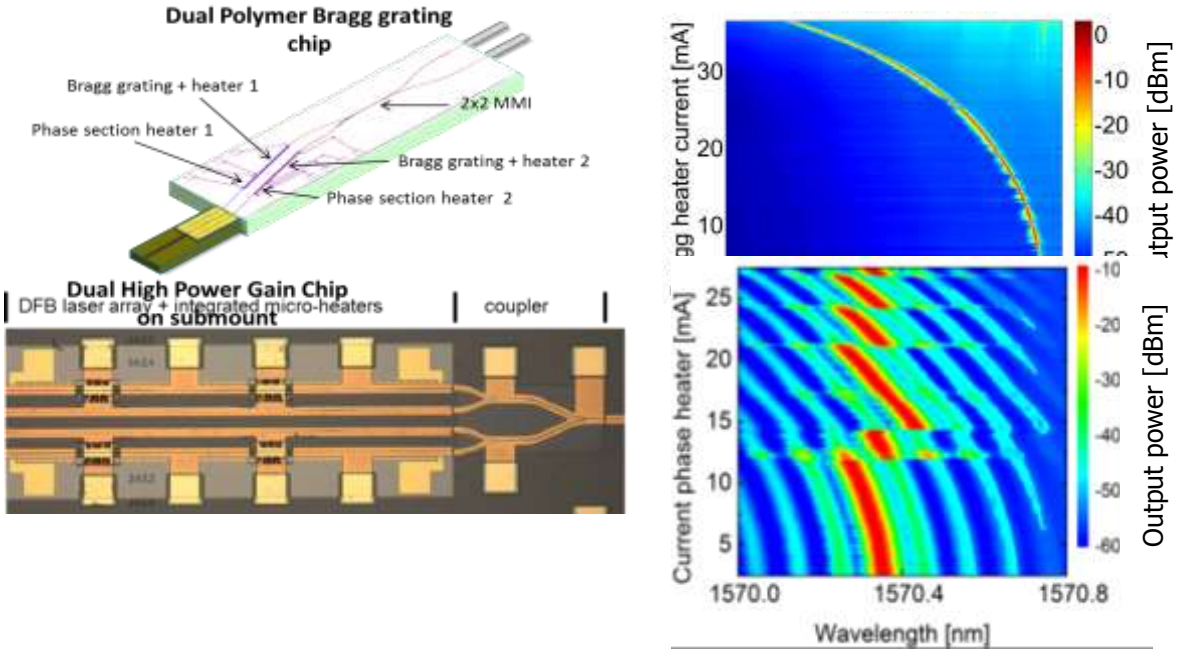



*Fig. 5: Hybrid integrated tunable cw-laser (top, left) and monolithically integrated tunable Quantum Dot (InP) cw-laser (bottom left). Bragg and phase section tuning of the hybrid laser (right)*

## Silicon Photonics

- Waveguide-integrated Ge photodiode with a 3dB-bandwidth of 70GHz and a responsivity of 1A/W

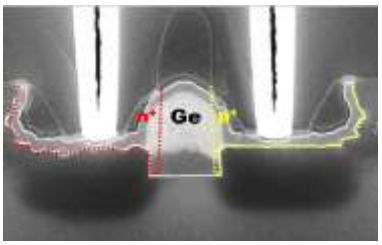



*Fig. 6: SEM cross section2nd generation Ge photodiode*

- 32Gbps travelling wave modulators

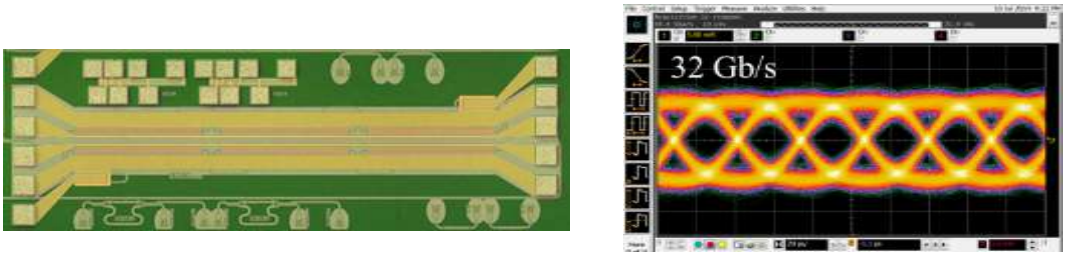



*Fig. 7: Chip picture of the travelling-wave modulator and 32Gbps eye diagram*

- Monolithic integration of Silicon Photonics and SiGe Electronics


*Fig. 8: Meandered modulator for 28Gbps operation co-integrated with high speed driver*

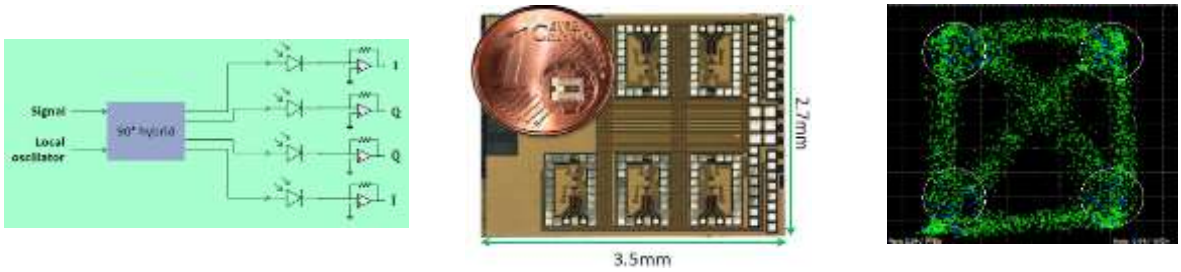



*Fig. 9: Fully monolithic integrated 56Gbps single-pol. coherent receiver in IHP photonic BiCMOS (SG25_EPIC). Schematic (left), chip picture (middle) and 56Gbps QPSK eye-diagram (right)*

**About the SASER Optical-Components sub-project:**

The horizontal cross-cutting project "SASER: Optical Components" started in September 2012 and finished its work in February 2016.

The consortium, led by Finisar, included 9 partners from Germany and the United Kingdom:

Finisar Germany GmbH, Germany
Fraunhofer Society – Heinrich-Hertz-Institute, Germany
IHP GmbH, Germany
Axenic, United Kingdom
RWTH Aachen – IPH, Germany
AMO GmbH, Germany
Technical University Berlin – HFT, Germany
University of Stuttgart – INT, Germany
University of Kassel – INA and CEP, Germany

For further information, please contact the coordinator andreas.steffan@finisar.com or visit the project website at: https://www.celticplus.eu/project-SASER/

## 2 Efficient Electronic Converters Sub-Project

The efficient electronic converter sub-project was a cross-functional-activity, working and partnering with all other SASER sub-projects. The sub-project was led by Socionext Europe GmbH (SNEU), which has been working with SASER-SaveNet, SASER-Siegfried, SASER-ADVAntageNet and other cross-functional projects such as optical components and reference scenarios, test infrastructures and system tests, see below Fig.10 for more details.

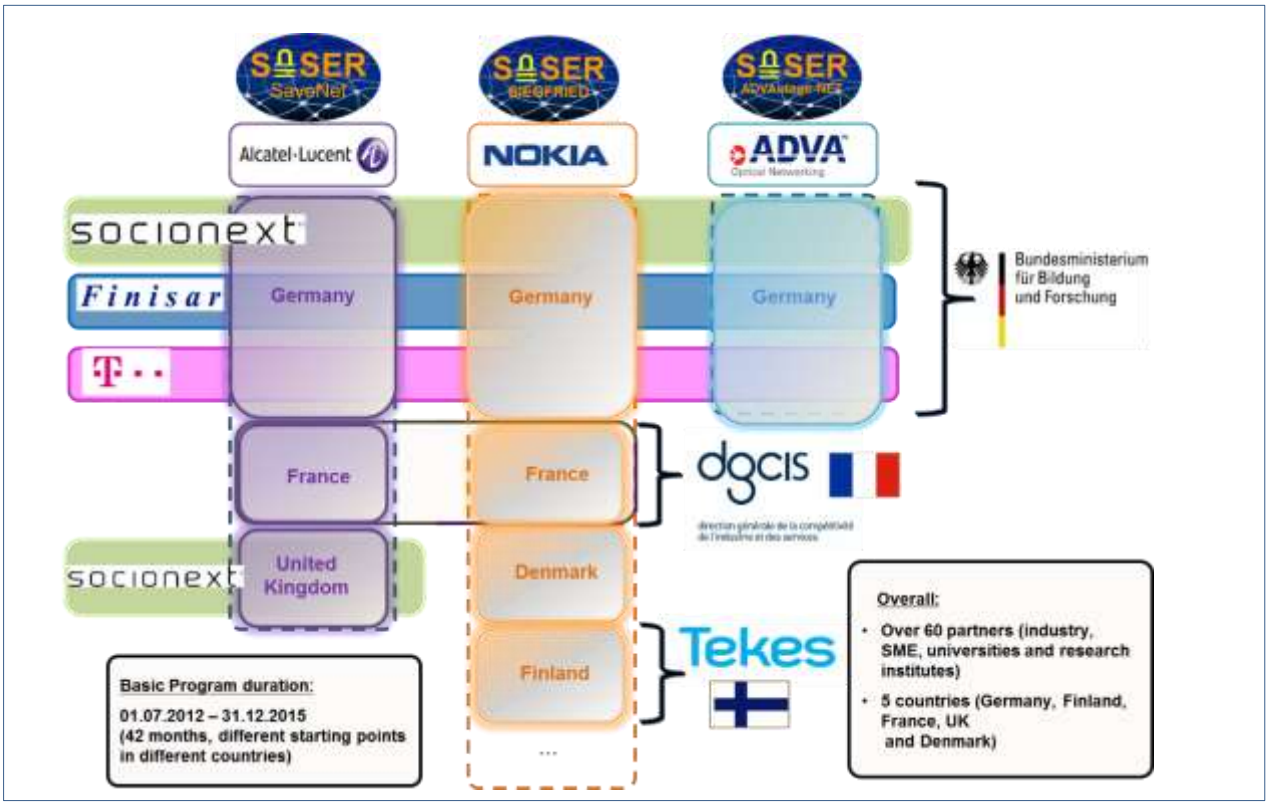



*Fig. 10: Overview/Structure of SNEU & Partners within SASER / Celtic Plus*

**Some of the main goals of SNEU for this program have been as follows.**

- Development of a complete Analog to Digital Converter (ADC) and Digital to Analog (DAC) family with different variants (incl. IPs, and macros that can be partly re-used).
- Investigation and manufacturing of a suitable high-end package solution.
- R&D of test chips and development kits (DKs) including SW and GUI and to help partners to bring-up the ADC/DAC solutions and test, validate, de-bug/optimize (incl. system solutions, field-trials).
- R&D on different types of modulation formats and systems implementation.
- Enabling R&D demonstrators and to help partners on the implementation of ADC/DAC solutions, incl. supporting and executing system tests and field trials.
- Manufacture test chips in standard 28nm CMOS technology, using new concepts and innovative solutions that can be successfully integrated into future telecom and transport networks.
- Ensure the outcome is beneficial to European businesses and marketplaces.

Main steps to achieve the above goals have been to generate a target specification with the partners to ensure that the required device and system parameters were satisfactory for R&D test, evaluation and optimization purposes. Once the target specification was finalized, the R&D work on the ADC/DAC test chip was completed in several iterations (see below Fig. 11), including the package development (further info given in Fig. 12).

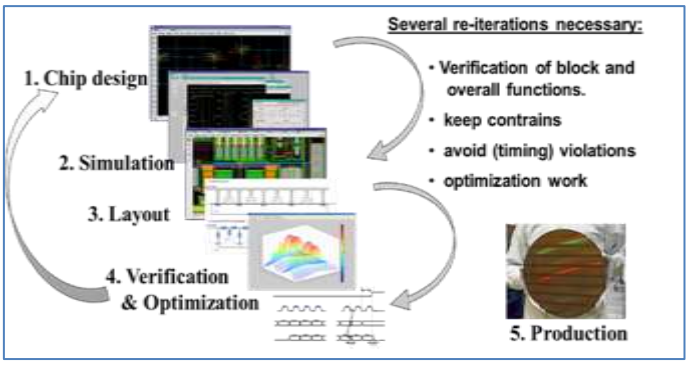



*Fig. 11: Basic iterative steps for R&D on ADC/DAC test chip*

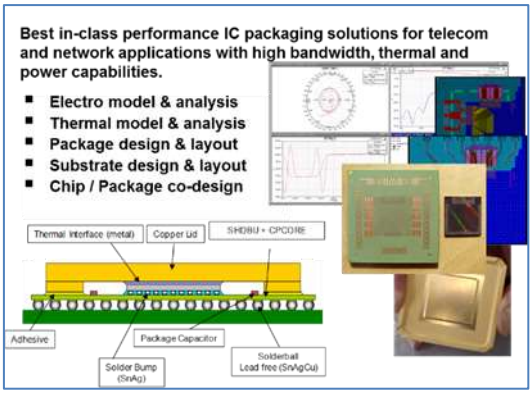



*Fig. 12: R&D activities on the package*

In parallel to the test chip and package activities the R&D for development kits (in the form of a PCB and ADC & DAC evaluation platform) was performed. Fig. 13 shows some of the main tasks performed and gives a basic block diagram and picture of the PCB.


*Fig. 13: Main tasks performed on the DK and basic block diagram and picture of the PCB.*

**Main deliverables by the SASER partners under the Celtic-Plus programme**

To provide innovative technical concepts and solutions for future telecommunication and transport networks. This required ultra-high speed, ADC/DAC solutions with very high energy efficiency that can be used for future R&D and integrated into new innovative systems, as well as future products.

SNEU undertook all necessary R&D work and manufactured a set of ADC/DAC test chips and Development Kits (DKs) including SW/GUI.

One deliverable has been to support the partners on start-up, measurements/test and assisting with debugging and optimization of possible demonstrators for extensive R&D work, system tests and planned field trials.

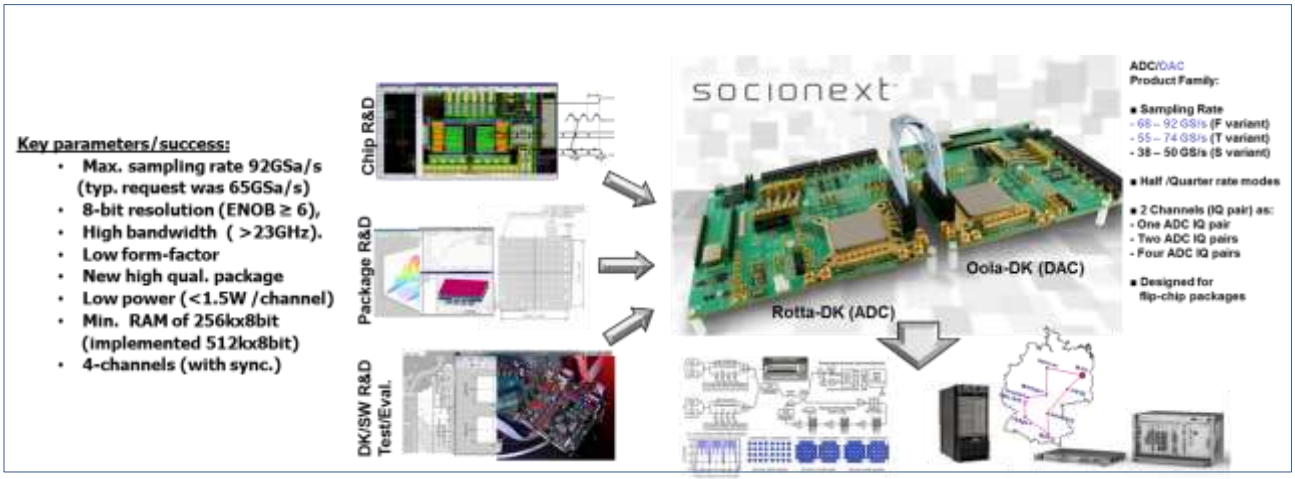


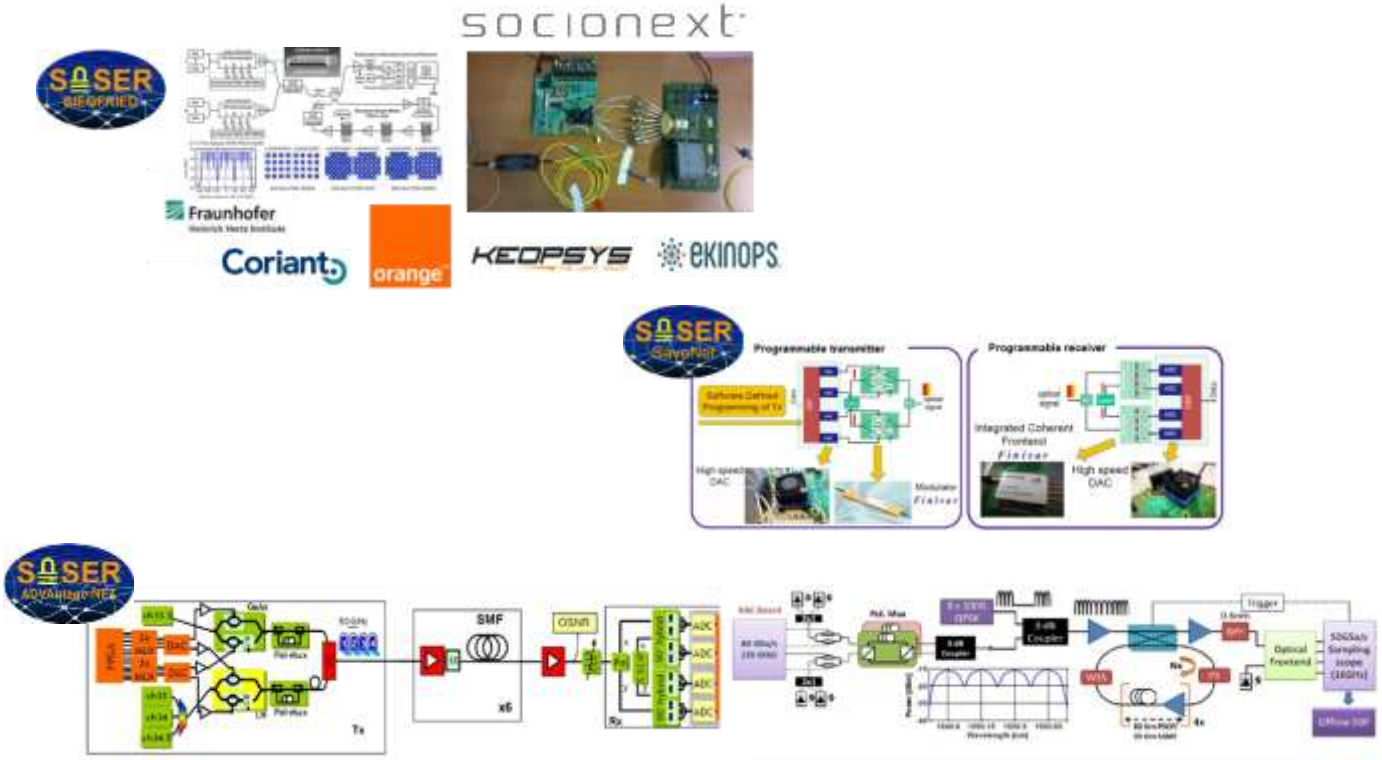

*Fig. 14: An overview on the deliverables (incl. some key parameters and ADC/DAC product family).*

**Key achievements of the "Efficient Electronic Converters" Sub-Project:**

- A family of state-of-the-art ADC/DAC has been developed, suitable for real product development.
- DKs have been manufactured/provided to partners
  → enabling chip and system tests / optimization.
- R&D on modulation formats & systems has been performed and built, and demonstrators/proto-types supported.
  → Outcome: over 40 publications from partners using ADC/DAC technology (additional support on 100Gb/s G.698.2 or ITU-T SG15 (G.sub39) spec. definitions).
- Several system tests and field trials with different partners were performed

**Key success stories of the "Efficient Electronic Converters" Sub-Project**

- The collaborative work of the partners was exceptionally good and the quality of the results obtained met all the program milestones and exceeds the overall expected achievements. This was key for successful design and implementation of real products that will be highly beneficial for new systems and infrastructures in the future.
- The technical results obtained have been very helpful for the R&D activities and can be used as basic guidelines for future product developments. The system know-how obtained increased the understanding for possible next generation implementations and will make decision making towards the right solution easier.
- Tests and field trials were performed.
  Result: Record-breaking Transmission Field Trial of 38.4 Tbps over 762 km Lyon-Marseille-Lyon Fiber Optic Link, or for example, a live demo during the Final SASER/Celtic+ Event.




- First developments for real products started including new concepts and innovative solutions for real future telecom & transport networks. This is possible due to a standard 28nm CMOS process being used. It enables the integration of multiple ADCs/DACs with tens of millions of gates of signal processing logic and memory on a single chip solution making implementations and competitive products possible. This new concept and innovative solution can be successfully integrated into real future telecom & transport networks for Germany & Europe.
- It is assumed that the 28nm ADC/DAC solutions will replace the existing 40nm ADC/DAC technology.

  The existing 100G solutions will be enhanced to next generation 500G/1Tb TX & RX telecommunication systems and networks.

**About the "Efficient Electronic Converters": sub-project:**

The horizontal cross-cutting project "SASER: Efficient Electronic Converters" started in August 2012 and finished its work in December 2015.

Socionext Europe GmbH (SNEU) has contributed to this `Efficient Electronic Converters' sub-project, which was partly funded by the German BMBF for the Celtic-Plus European Flagship Project SASER (Safe and Secure European Routing).

SNEU is a leading provider of next generation System-on-Chip (SoC) solutions. Born from the system LSI businesses of Fujitsu and Panasonic, Socionext launched globally in March 2015. SNEU focuses on imaging and network solutions, with an emphasis on the automotive and optical networking markets, as well as Custom SoC solutions for other areas which include consumer and industrial applications.

SNEU has been working with the other horizontal and cross-section SASER sub-project partners to enable R&D activities for future safe and secure high speed data networks including the optimization of components/system solutions.

For further information please contact Tomislav.Drenski@socionext.com or visit the project website at: https://www.celticplus.eu/project-SASER/

## 3 Test Infrastructure and System Tests Sub-Project

Deutsche Telekom T-Labs contributed to the SASER project with the horizontal cross-sectional sub-project entitled “Test Infrastructure and System Tests”, which was partly funded by the German BMBF (16BP17200).

A research and development test network infrastructure including a countrywide German 2,100 km long bidirectional fiber ring was set-up using an Alcatel-Lucent 1626 LM system, shown in Fig. 15. This R&D test network infrastructure provides and enables flexible and simultaneous test scenarios for every aspect of components and integrated systems including multi-vendor interoperability, multi-layer interworking, software defined networking, network function virtualization, network management functionalities, resilience, and security.


*Fig. 15: Countrywide German 2,100 km long bidirectional R&D test network fiber infrastructure*

Various test activities were performed, demonstrating the feasibility of the provided network architecture and the high speed and high performance connectivity. Optical 12x12 port AWG (arrayed waveguide grating) devices with 400 GHz bandwidths are used as multi-functional devices supporting bidirectional operation, passive optical wavelength routing, and OADM (optical add/drop multiplex) functionality to connect different DWDM systems, thus demonstrating transparent optical multi-vendor DWDM interworking.

Based on the R&D test network infrastructure, together with T-Systems and various partners, Tbit/s transmissions and high performance computing applications were demonstrated between the high performance computing (HPC) centres of the Universities of Dresden and Stuttgart, 1,000 km apart. The connections to the fiber-ring are provided using ADVA FSP3000 DWDM systems, connected to the ring-nodes in Leipzig and Stuttgart, respectively. Increased spectral efficiency, passive wavelength routing, and multi-vendor optical interworking between ADVA and Alcatel-Lucent DWDM systems were demonstrated simultaneously.

Flexible optical bandwidths of 3 x 33 GHz and 10 x 50 GHz channels for simultaneously transmitted 100 Gbit/s signals are depicted in Fig. 16, demonstrating DWDM channel interworking of 100 Gbit/s signals over 1,000 km and 3 bit/s/Hz spectral efficiencies resulting in 14.4 Tbit/s link capacities, relevant for next generation optical transport networks, elastic optical channels, and flexible grids.

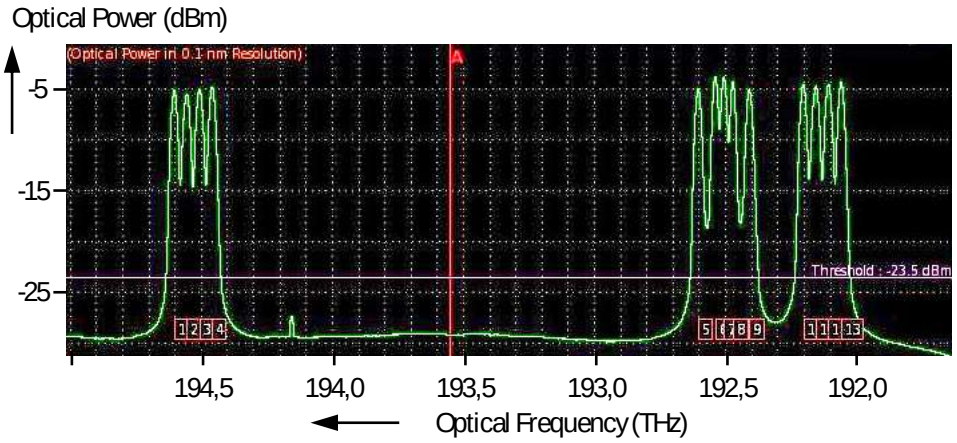



*Fig. 16: Simultaneously transmitted 13 x 100 Gbit/s signals via 10 x 50 GHz and 3 x 33 GHz DWDM channels, received after 1000 km real transmission between high performance computing centres of the technical universities of Dresden and Stuttgart*

In the HPC centres, Brocade and Intel Security Technologies are used to perform Tbit/s generation and processing including software defined networking and network virtualization functionalities.

In particular, 1-Tbit/s high performance computing (HPC) applications via long haul transmission of 1,000 km between HPC data centers of ZIH (Zentrum für Informationsdienste und Hochleistungsrechnen) in Dresden and HLRS (Höchstleistungs Rechenzentrum Stuttgart) in Stuttgart were demonstrated. Link saturation of the 1 Tbit/s connection was demonstrated live during the SuperComputing 2014 conference in New Orleans, as shown in Fig.17.

*Fig. 17: Live demonstration at the SuperComputing 2014 conference in New Orleans of 1 Tbit/s transmission via 1000 km distance connecting high performance supercomputing centres of the technical universities of Dresden and Stuttgart.*

Scientific HPC applications of various domains were bandwidth-wise orchestrated using SDN-based QoS profiles. Network function virtualization (NFV) functionality of multi-thread capable virtualized firewalls was demonstrated to fully support 40 Gbit/s 8k jumbo frames using only one core.

For further information please contact Ralf-Peter.Braun@telekom.de, visit the project website at https://www.celticplus.eu/project-SASER/ or see the invited paper at the OECC 2015 in Shanghai. R.-P. Braun et al., “Tbit/s 1000 Km Field Trial, Achieving Increased Spectral Efficiency, SDN Enabled Application Traffic, and Passive Wavelength Switching”, invited paper, OECC 2015, paper JMoA.31.