



## CELTIC-NEXT PROPOSERS BROKERAGE DAY

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# MicroLink

## Blue MicroLED Optical I/O

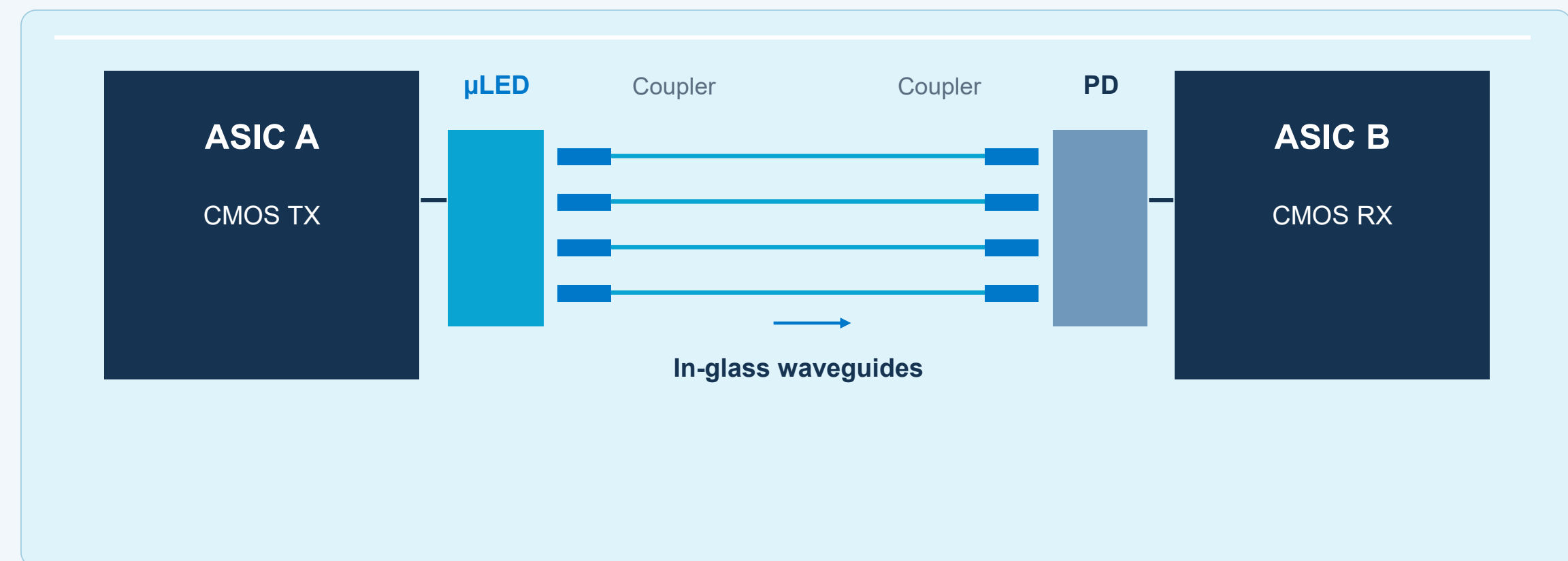
From fiber bundles  
to glass interposers

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### THE STRATEGIC DESTINATION



**A working two-ASIC glass-interposer POC**

**36-MONTH CONSORTIUM PROPOSAL**

## Make optical I/O an integrated micro-device platform.

The objective: lower complete-link energy, higher I/O density and a smaller integration footprint.

### MAIN BENEFIT

#### Efficient, compact optical I/O

Co-design the emitter, optics, CMOS and receiver around the energy of the complete link.

### ADDED VALUE

#### VueReal device-to-system IP

Custom epitaxy, a semipolar development route, MIS sidewall engineering and MicroSolid Printing.

### WHY PARTICIPATE

#### Build reusable technology

Co-develop two working demonstrators and the process, circuit and packaging blocks behind them.

**FIBER-BUNDLE DEMONSTRATOR**



**GLASS-INTERPOSER PROOF OF CONCEPT**

## VueReal: IP, people and a platform to execute.

**600+**

Patent applications

**225+**

Patents

**USD \$100M+**

Funding

**50+**

Employees

### Operational production facility

MicroSolid Printing™ mass-transfer technology, scalable manufacturing and an innovation-driven culture.

### MicroLED technology milestones

Industry-first 4K MicroLED at 6,000 PPI.  
World's first MicroLED reference design kits.

**Proposed optical I/O extends VueReal's micro-device and integration capabilities into a new application.**

## Differentiated emitters. A practical fiber-bundle route.

### 01 Custom epitaxy IP

AR1: speed-led. AR2: efficiency-led.  
Tune carrier lifetime and optical output.

### 02 Semipolar approach

Reduce polarization fields to improve  
carrier overlap and the speed-efficiency trade-off.

### 03 MIS: active sidewall field control

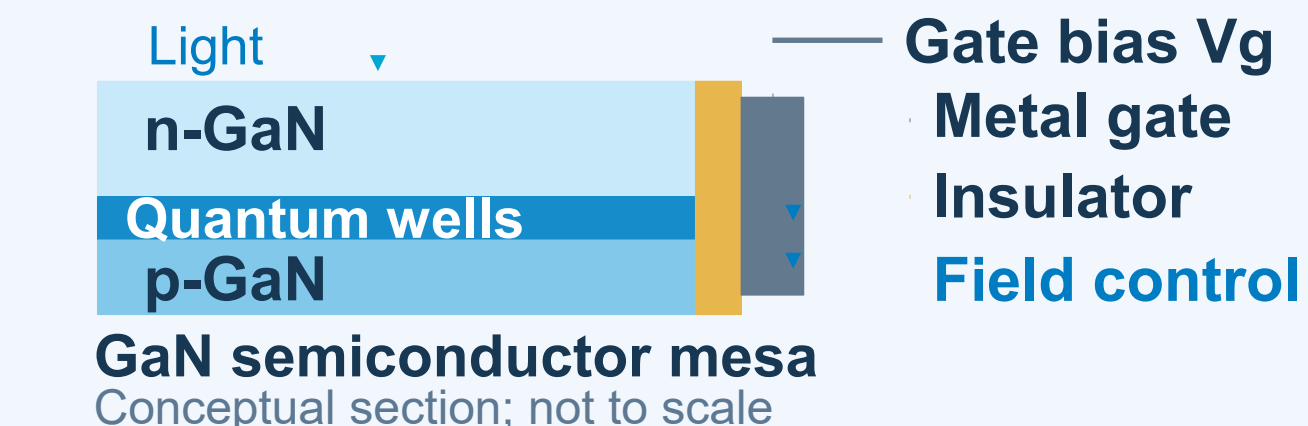
#### Metal-insulator-semiconductor

A separately biased metal gate sits over an  
insulating film on the GaN sidewall. Its field  
changes local carrier density and can reduce  
trap-assisted, non-radiative losses.

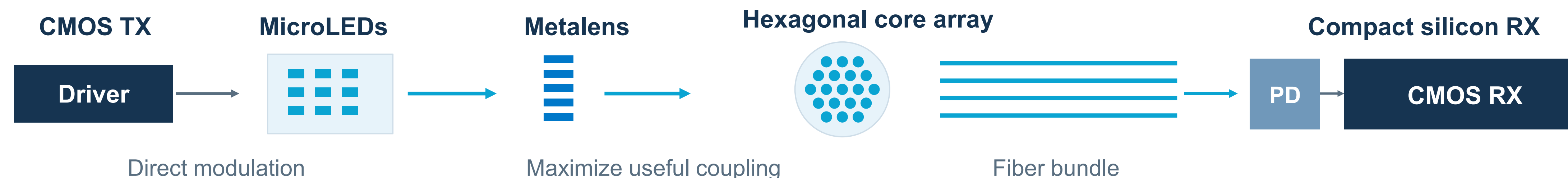
**Aim: preserve efficiency as emitters shrink.**

Validate MIS efficiency, capacitance, leakage and modulation response together.

#### LOCAL SIDEWALL DETAIL



### STREAM 1 | METALENS-COUPLED FIBER BUNDLE



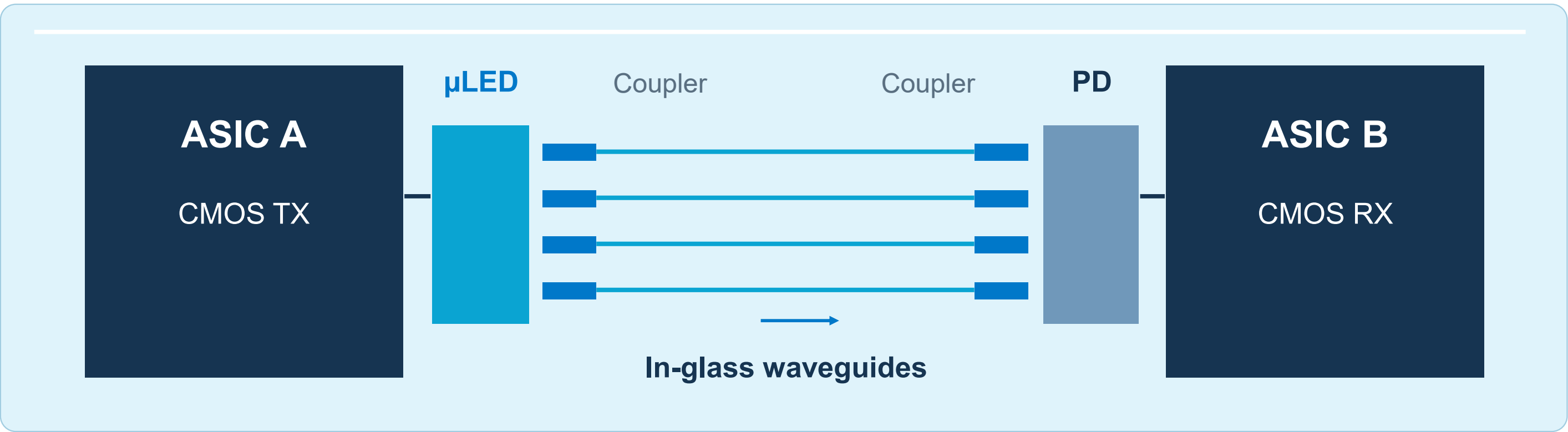
After Si removal: contacts to CMOS; emission from the exposed n-GaN side.

**Select variants by measured complete-link energy, not LED efficiency alone.**

# The future direction: optical routing inside the glass interposer.

Deliver a working two-ASIC optical link — not only a simulation or a passive coupon.

TWO ASICs IN ONE GLASS INTERPOSER



Local hybrid-bonded interfaces | Parallel lanes | Top view

## WHY THIS IS INNOVATIVE

### Optics inside the package

Directly modulated emitters connect ASICs through in-glass routing.

### Device-to-package co-design

Custom epi, MIS, CMOS, hybrid bonding and coupling are optimized together.

### Dense parallel I/O

Scale through arrays of optical lanes, with short local electrical interfaces.

## 36-MONTH EXECUTION PLAN

### M1–6 Co-design

Link budget + interfaces

### M7–15 Build test vehicles

Epi, CMOS + glass coupons

### M16–24 Integrate + prove

Hybrid bonding + fiber link

### M25–36 Glass POC

Two-ASIC link + validation

## Seeking a semiconductor + photonics integration partner.

An open consortium led by a Canadian technology proposer; complementary growth partners welcome.

### VUEREAL

Proposer | Canada

Custom epitaxy  
Custom MicroLED  
MicroSolid Printing  
Emitter + system  
concept

#### PROCESSING + HYBRID BONDING

Die-to-wafer / wafer-to-wafer bonding;  
CMP, alignment, thin-film processing and  
yield metrology.

#### CMOS DESIGN + HIGH-SPEED TEST

Low-energy TX drivers, compact RX/TIA,  
ASIC tape-out, packaging and electrical  
link characterization.

#### OPTICS + GLASS INTEGRATION

Blue-compatible in-glass waveguides,  
couplers, metalens design, optical  
packaging and link metrology.

#### CUSTOM EPITAXY FOUNDRY

MOCVD growth of VueReal-designed  
GaN/InGaN stacks; semipolar  
development and materials  
characterization.

European and international partners sought. No additional consortium member is represented as confirmed.

# Let's build the glass-interposer proof of concept.



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**Hybrid bonding | CMOS design | Optical integration | Custom epitaxy**